FIG. 1

Logic Analyzer 100

Computer Platform 101

| DATA STORAGE UNIT(S) 165 |
| SYSTEM MEMORY 104 |
| Processor 102 |
| Windows / OS 114 — GUI 116 |
| I/O Cards 106 |
| Keyboard 108 |
| Pointing Device 110 |

Bus 120

Video Display Cntrl 122 → Display 112

Logic Analysis Module 140
Trigger Manager 180

Signal Data Memory 142

Signal Acquisition Module 122

Switch 136
Buffer 132
Signal Data 154
Switch Control 155
Signal Data 154
Trigger Scavenger 134
Trigger Specification 150
Data Sampling Detector 138
Logic Signals 152

Device Under Test (DUT) 131

Channels 130

Figure 2

TRIGGER MANAGER 180

Signal Acquisition Module 122

TRIGGER SEQUENCER 202

TRIGGER Development Subsystem 204

TRIGGER SEQUENCES 205

TRIGGER Definition 211

TRIGGER Controls 207

(TRIGGER CONTROLS) 207

TRIGGER Definition 20A

SHARED TRIGGER SPEC 223

Run Acquisition 215

Run/Halt Trigger

SAVE TRIGGER SPEC 217

SAVE + RECALL Subsystem 208

AUTO

Current TRIGGER Specification 213

SHARED TRIGGER SPEC 219

SYSTEM MEMORY 104

TRIGGER CONTROLS Subsystem 206

TRIGGER Controls 207

COUNT QUALIFICATION 227

SAMPLE RATE 229

MEMORY DEPTH 231

TRIGGER POSITION 233

Windows/ Operating System 114 w/ Graphical User Interface 115

TRIGGER Specification Display + Control 245

selected TRIGGER Controls

TRIGGER SPECIFICATION 150

Fig 3

340 (serial inputs)

340 (LAN ports)

320 (line card)

315 (ASICS)

380 (parallel data busses)

301 (line card)

390

BACK PLANE FABRIC

LOGIC ANALYZER
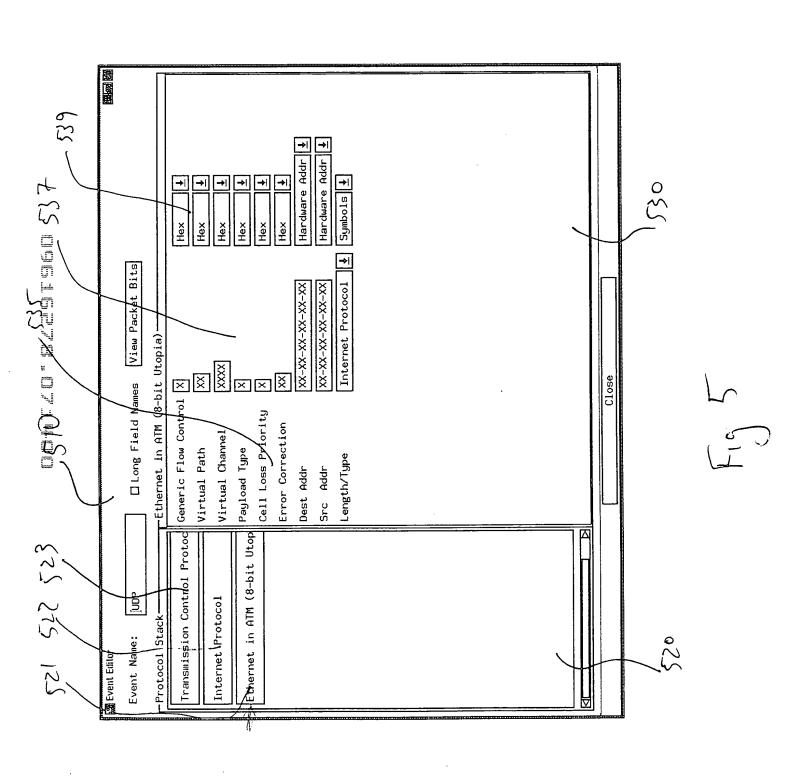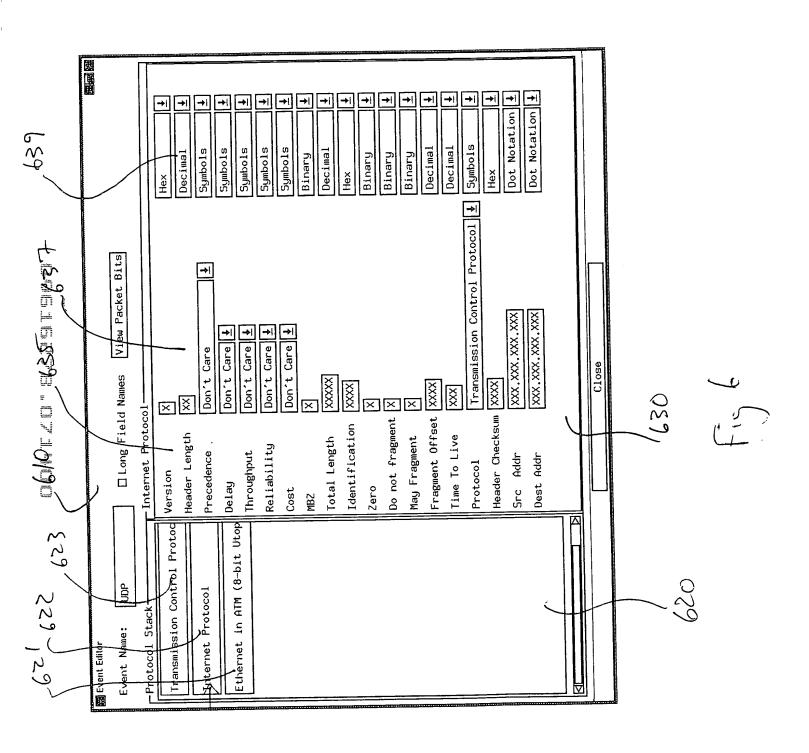
370

385

Destination Address: 48 bits: 1 1-XX-XX-1 1-XX-XX-XX
Source Address: 48 bits: XX-XX-XX-XX-XX-XX-XX
Length/type: 16 bits: XXXX

Fig. 4a

Data Bit Block	Don't Care Mask
11	00
00	ff
00	ff
11	00
00	ff
00	ff
00	ff
00	ff
00	ff
00	ff
00	ff
00	ff
00	ff
00	ff

Fig. 4b

Destination Address: 48 bits: XX-XX-XX-1 1-XX-XX-XX
Source Address: 48 bits: XX-XX-XX-XX-XX-XX-XX
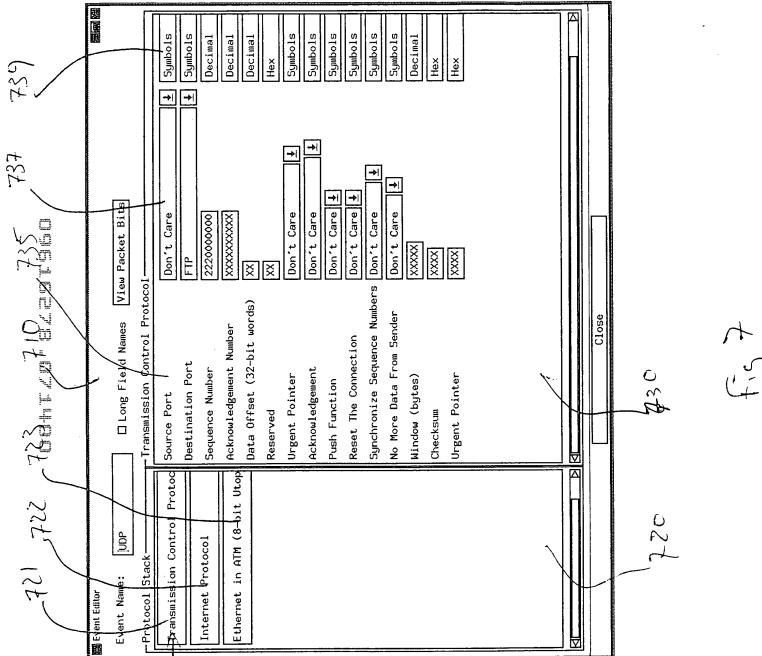Length/type: 16 bits: 0800

Fig. 4c

Data Bit Block	Don't Care Mask
11	00
00	ff
00	ff
11	00
00	ff
00	ff
00	ff
00	ff
00	ff
00	ff
00	ff
00	ff
08	00
00	00

Fig. 4d

Event Editor

Event Name: [UDP]

Protocol Stack
Transmission Control Protocol
Internet Protocol
Ethernet in ATM (8-bit Utopia)

☐ Long Field Names   View Packet Bits

Ethernet in ATM (8-bit Utopia)

Generic Flow Control [X]   Hex [↓]
Virtual Path   [XX]   Hex [↓]
Virtual Channel   [XXXX]   Hex [↓]
Payload Type   [X]   Hex [↓]
Cell Loss Priority   [X]   Hex [↓]
Error Correction   [XX]   Hex [↓]
Dest Addr   [XX-XX-XX-XX-XX-XX]   Hardware Addr [↓]
Src Addr   [XX-XX-XX-XX-XX-XX]   Hardware Addr [↓]
Length/Type   [Internet Protocol] [↓]   Symbols [↓]

Close

Fig 5

Event Editor

Event Name: [ ]

Protocol Stack
| Transmission Control Protocol |
| Internet Protocol |
| Ethernet in ATM (8-bit Utop |

UDP

☐ Long Field Names   View Packet Bits

Internet Protocol

Version	X		Hex
Header Length	XX		Decimal
Precedence	Don't Care	↓	Symbols
Delay	Don't Care	↓	Symbols
Throughput	Don't Care	↓	Symbols
Reliability	Don't Care	↓	Symbols
Cost	Don't Care	↓	Symbols
MBZ	X		Binary
Total Length	XXXXX		Decimal
Identification	XXXX		Hex
Zero	X		Binary
Do not fragment	X		Binary
May Fragment	X		Binary
Fragment Offset	XXXX		Decimal
Time To Live	XXX		Decimal
Protocol	Transmission Control Protocol	↓	Symbols
Header Checksum	XXXX		Hex
Src Addr	xxx.xxx.xxx.xxx		Dot Notation
Dest Addr	xxx.xxx.xxx.xxx		Dot Notation

Close

Fig 6

Event Editor

Event Name: UDP

Protocol Stack
- Transmission Control Protoc
- Internet Protocol
- Ethernet in ATM (8-bit Utop

☐ Long Field Names | View Packet Bits |

Transmission Control Protocol

Source Port	Don't Care →	Symbols
Destination Port	FTP →	Symbols
Sequence Number	2220000000	Decimal
Acknowledgement Number	XXXXXXXXXX	Decimal
Data Offset (32-bit words)	XX	Decimal
Reserved	XX	Hex
Urgent Pointer	Don't Care →	Symbols
Acknowledgement	Don't Care →	Symbols
Push Function	Don't Care →	Symbols
Reset The Connection	Don't Care →	Symbols
Synchronize Sequence Numbers	Don't Care →	Symbols
No More Data From Sender	Don't Care →	Symbols
Window (bytes)	XXXX	Decimal
Checksum	XXXX	Hex
Urgent Pointer	XXXX	Hex

Close

721 722 723 728 710 732 735 735 737 739

720 730

Fig 7

Analyzer<D> – 333MHz State/2GHz Timing Zoom 2M Sar

File   Window   Edit   Options   Clear   Help

Sampling | Format   Trigger | Symbol |
Trigger Sequence

```
1  FIND PACKET
   1.1  If TxSOP = 1 Binary
        occurs 1 time
        then Goto 1.2
   1.2  If Anything
        occurs 5 times consecutively
        then Goto 1.3
   1.3  If TxDATA = 0000100000000000  Binary
        occurs 1 time
        then Goto 1.4
        Else if Anything
        then Goto 1.1
   1.4  If Anything
        occurs 4 times consecutively
        then Goto 1.5
   1.5  If TxDATA = XXXXXXX00000001  Binary
        occurs 1 time
        then Goto 1.6
        Else if Anything
        then Goto 1.1
   1.6  If Anything
        occurs 1 time
        then Goto 1.7
   1.7  If TxDATA = 0000101100001011  Binary
        occurs 4 times consecutively
        then Trigger and fill memory
        Else if Anything
        then Goto 1.1
```

Help   Close

FIG 8b

Event #1 – Packet

```
   0.......8....15
0  XXXXXXXXXXXXXXXX
1  XXXXXXXXXXXXXXXX
2  XXXXXXXXXXXXXXXX
3  XXXXXXXXXXXXXXXX
4  XXXXXXXXXXXXXXXX
5  XXXXXXXXXXXXXXXX
6  0000100000000000
7  XXXXXXXXXXXXXXXX
8  XXXXXXXXXXXXXXXX
9  XXXXXXXXXXXXXXXX
10 XXXXXXXXXXXXXXXX
11 XXXXXX00000001
12 XXXXXXXXXXXXXXXX
13 0000101100001011
14 0000101100001011
15 0000101100001011
16 0000101100001011
17 XXXXXXXXXXXXXXXX
18 XXXXXXXXXXXXXXXX
```

Close

FIG 8a